

## **REMARKS**

Reconsideration of the application is respectfully requested in view of the Applicant's remarks. The Office Action has rejected claims 2, 6, and 8-13.

Claims 2, 8, 9, and 10, have been amended. No new matter has been added.

### **Rejections under 35 U.S.C. §103**

Claims 2, 6, and 8-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Song et al (Song, O; Menon, P. R.; Parallel pattern fault simulation based on stem faults in combinational circuits, Proceedings International Test Conference, Sept. 10-14, 1990, pp 706-11) [hereinafter referred to as "Song"] and in view of U.S. Patent No. 6205567 to Maruyama ("Maruyama"). Applicant respectfully traverses the rejection. In accordance with M.P.E.P. § 2142, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met." (M.P.E.P. § 2143.) First, some suggestion or motivation in the prior art references or in the knowledge of one of ordinary skill in the relevant art must exist to modify or combine the references. Second, if the references are combined, a reasonable expectation of success must be shown. Then, finally, all of the claim limitations must be taught or suggested by one reference or a combination of references. To establish a *prima facie* case of obviousness based on a single reference that does not teach all the elements of a claim, the Examiner must provide a rationale for modifying the teachings of the reference. See *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000), citing, *B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp.*, 72 F.3d 1577, 1582, 37 U.S.P.Q.2d 1314, 1318 (Fed. Cir. 1996).

Song discloses a method for improving the speed of fault simulation of combinational circuits by performing parallel pattern single fault simulation (PPSFP) wherein a number of test patterns are processed simultaneously based on the word size of the host machine being used to perform the fault simulation. Paragraph 1, Col. 2, page 706. In addition, Song discloses a "method for reducing the expense of backtracing by identifying lines where backtracing may be stopped." Abstract, Col. 1, page 706.

Applicant initially notes that Song does not teach identifying potential faults to be tested by the test by backtracing "in a single detection pass," as is required by claims 2, 8, 9, and 10. Instead Song requires that two separate backtracing steps be performed as part of the PPST algorithm to determine the faults. The algorithm disclosed in Song is replicated below:

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For every set of test patterns,  
    Perform true-value simulation.  
    For every active (i.e. undropped) FFR,  
        Backtrace from its stem (PO) upto FOB's or PI's  
        Propagate the stem fault to a PO, if necessary  
        If any stem fault is detected  
            Backtrace from the stem, collecting detection information  
            If all faults in the FFR have been detected  
                Drop the FFR  
End  
[Col. 2, Page 707 – Col. 1, Page 708, emphasis added].
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Song discloses the performance of two separate backtracing steps, such that "[t]he set of faults detected by a set of test patterns is determined by a second backtracing inside FFR's." Paragraph 4, Col. 1, Page 708. Thus, Song discloses the performance of a first and second backtracing step (Paragraph 1, Col. 2, Page 708), and therefore does not teach or suggest identification of the potential faults to be tested by the test by backtracing "in a single detection pass" as is required by claims 2, 8, 9, and 10.

The Examiner asserts that "Song teaches that a first backtracing is performed to detect stem-critical fault values and that a second backtracing is performed to .... gather information about the faults that were detected in the first backtracing." Office Action, mailed August 18, 2006, page 3. The Examiner also asserts that "Song teaches identifying potential stem-critical faults to be tested by the test by a first backtracing, in a single detection pass occurring during the first backtracing." Office Action, page 3. Applicant respectfully disagrees with the Examiner and submits that the faults are identified in Song **only after** the second backtracing is performed to gather information about the faults that were detected in the first backtracing. The Examiner's assertion is also contrary to the teaching in Song that "[t]he set of faults detected by a set of test patterns is determined by a second backtracing inside FFR's." Paragraph 4, Col. 1, Page 708.

Finally, Applicant notes that Song does not disclose backtracing in a single detection pass *through logic gates and memory elements*, as required by all claims. Song only discloses performing the disclosed backtracing through combinational logic and, contrary to the Examiner's assertions, does not teach or suggest backtracing through both logic gates *and* memory elements. The Examiner asserts that the backtracing in Song is for testing combinational logic but . cites to the "last sentence in the second column of page 706 in Song" as indicating a delay in backtracing that according to the Examiner can "only be attributed to memory elements required for interconnecting various combinational elements". Office Action, page 3. Applicant respectfully disagrees with the Examiner's assertions. Applicant submits that combinational logic is understood by one of ordinary skill to be a type of logic circuit having no memory such that an output of the combinational logic circuit is a function of the present input only. The text and the figures in Song are consistent with this ordinary meaning of

combinational logic and therefore do not support the Examiner's assertion. Applicant further asserts that such delays commonly occur in combinational logic gates and the fact that delay is present has absolutely no bearing on whether memory is present in Song. There simply is no such teaching regarding memory elements in Song. Finally, Applicant also notes that the last sentence on page 706 of Song merely states that multiple sets of test patterns are applied in Song, and contains no disclosure of backtracing in a single detection pass through logic gates *and* memory elements. Therefore, Applicant respectfully submits that Song contains no teachings relating to backtracing through memory elements.

The Examiner asserts that Maruyama "teaches use of a good machine simulation on the IC having logic gates and memory elements." Page 4, Office Action mailed April 10, 2006. The Examiner provides no citation for such a teaching, and Applicant studied Maruyama and cannot find any disclosure in Maruyama of either "performing a good machine simulation on the IC to values of each internal node of the IC," or of performing such a good machine simulation on an IC having memory elements. First, Maruyama only discloses the use of true-value simulation to determine whether there is "a difference between the propagated fault and the result of the true-value simulation" at an observation point. Maruyama, Col. 12, lines 18-24. Second, Maruyama defines an activation path *between* circuit branch points, which ultimately end at either memory elements, circuit inputs, or circuit outputs. Maruyama does not try to identify faults across memories in a single detection pass. Maruyama, Col. 12, lines 31-40.

Based on the forgoing, Applicant respectfully submits that neither Song nor Maruyama either alone or in combination, teach or suggest any of the limitations discussed above, and therefore, claims 2, 8, 9, and 10 are allowable. Claim 6 depends from claim 2, claim 11 depends

from claim 8, and claims 12-13 depend either directly or indirectly from claim 9, and are therefore allowable for at least the same reasons.

Applicant would also like to note that the Attorney Docket No. was changed when the current attorney took over prosecution of this matter. Applicant requests that the Patent Office change their records to reflect this new reference number which is 700693-4011.

**Conclusion**

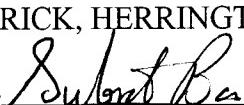
In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (650) 614-7669. If there are any additional fees required, please charge Deposit Account No. 15-0665.

Respectfully submitted,

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